ENHANCED ZIP LOAD MODELLING FOR THE ANALYSIS OF HARMONIC DISTORTION UNDER CONSERVATION VOLTAGE REDUCTION

Gareth MCLORN
Queen's University Belfast – U.K.
gmclorn02@qub.ac.uk

John MORROW
Queen's University Belfast – U.K.
dj.morrow@qub.ac.uk

David LAVERTY
Queen's University Belfast – U.K.
david.laverty@qub.ac.uk

Robert BEST
Queen's University Belfast – U.K.
r.best@qub.ac.uk

Xueqin LIU
Queen's University Belfast – U.K.
x.liu@qub.ac.uk

Seán MCLOONE
Queen's University Belfast – U.K.
s.mcloone@qub.ac.uk

ABSTRACT

Static load models, including ZIP coefficients, are an established facet of power systems modelling. Despite the rising penetration of non-linear load types across modern networks, the characterisation of load behaviours by such means remains effective. However, the accuracy of ZIP load based methods is shown to decline in the midst of high levels of harmonic current and/or voltage distortion. This observation is validated by making reference to the definitions set out in IEEE standard 1459-2010. Various power systems optimization strategies, such as Conservation Voltage Reduction, rely on load models to faithfully reproduce network conditions in simulation. Thus, an extension to the conventional ZIP model approach is proposed, which incorporates the effects of harmonic current distortion, attributable to particular load types, and harmonic voltage distortion.

INTRODUCTION

Since the 1970s, Conservation Voltage Reduction (CVR) has been promoted as a potential instrument for reducing electricity demand in power networks [1]. Contemporary research [2], [3] and [4] continues to endorse the technology for addressing some of the immediate and future challenges of power distribution. It is argued that the reduction of service level voltages can enhance the efficiency of customer appliances, decrease network losses, and increase the hosting capacity available to Low Carbon Technologies (LCTs) within modern networks.

Many of the benefits anticipated from CVR are contingent upon being able to predict the behaviours of different load types, as they respond to applied variations in service level voltage. Characterising loads as functions of applied voltage is commonly achieved through the use of static load models, of which the ZIP model is a noted example. A set of scalar ZIP coefficients is obtained for a load of interest from its three main voltage response characteristics: constant impedance (Z), constant current (I) and constant power (P) [5]. In the equations that follow for active (P) and reactive (Q) power, each coefficient denotes the degree of voltage sensitivity attributable to that response type. P_0 and Q_0 denote the active and reactive draws at nominal voltage, V_0.

$$P(V) = P_0 \cdot \left[Z_p \cdot \left(\frac{V}{V_0}\right)^2 + I_p \cdot \left(\frac{V}{V_0}\right) + P_p \right] \quad (1)$$

$$Q(V) = P_0 \cdot \left[Z_q \cdot \left(\frac{V}{V_0}\right)^2 + I_q \cdot \left(\frac{V}{V_0}\right) + P_q \right] \quad (2)$$

Equations (1) and (2) are key in the evaluation of CVR, especially in light of the sustained uptake of constant power type loads within modern networks [6]. Consider incandescent lighting; once regarded as the archetypal constant impedance load, and thus conducive (in terms of power savings) to the application of CVR. In recent years this load type has gradually been displaced by low wattage substitutes, such as Compact Fluorescent Lamps (CFLs) and Light Emitting Diode (LED) luminaires [7]. These device types are typically observed to exhibit almost constant power consumption across the permissible supply voltage range. The ensuing shift in aggregated load patterns, from constant impedance towards constant power type behaviours, is argued to increase line losses and thus negate some of the perceived benefits of CVR within distribution networks.

While this hypothesis is broadly accurate, it discounts the notion that the classic ZIP load model, of the manner presented in (1) and (2), remains incomplete. To comprehensively capture the impact of voltage variation upon load performance, the influences of harmonic current and voltage distortion need to be factored. In the context of IEEE 1459-2010 [8], additional metrics for power exist beyond the conventional representations for P and Q espoused by (1) and (2). Moreover, in literature within which the ZIP coefficients for various customer appliances are identified, the effects of harmonic distortion on the findings tend not to be discussed [5], [9].

Constant power attributes are increasingly synonymous with heightened levels of Total Harmonic Current Distortion (THD_I). This includes those appliances that couple with the power network through an intermediary AC to DC converter stage, such as electronic chargers for laptops, mobile phones, other portable devices and modern luminaires. Thus, one might consider how the underlying composition of the currents drawn by such loads adapt as terminal voltage is lowered, whereby the voltage response characteristics attributable to individual harmonic currents may be observed to differ across the harmonic spectrum. Indeed, some preliminary investigation of CFL and LED fixtures concludes that while the application of CVR may result in higher fundamental and root-mean-squared (rms) currents, this can coincide with a simultaneous decrease in THD_I [10]. In keeping with the relaxed THD_I constraints that apply to low-powered, Class C devices in [11], the harmonic currents measured for some of the devices in [10] are shown to be substantial. As such, it is reasonable to infer that their overall voltage-response characteristics are likely to be heavily influenced by factors that are not accommodated within the ZIP models introduced in (1) and (2). The potentially adverse impact of large-scale CFL adoption on network losses is a noted concern of [12].

This paper sets out an updated modelling approach, consisting of two strands, within which the impact of CVR on technical losses may be re-defined to encompass additional concerns related to harmonic distortion. Firstly, it is argued that the THD_I ratio that is attributed to a load can be modelled as a function of applied voltage, in the style of the ZIP models presented in (1) and (2). Secondly, the overall definition for apparent power (S) [8], in which the effects of THD_I and Total Harmonic Voltage Distortion (THD_V) are considered, ought to be used when gauging the impact of CVR on network current flows and associated losses.

Weaknesses inherent within classical interpretations of ZIP load modelling are shown to be satisfactorily resolved in circumstances where the applied level of harmonic pollution falls within existing power quality guidelines [13]. Moreover, a suitable linear approximation exists through which the flow of distortion powers can be resolved with an acceptable degree of accuracy. This hypothesis is validated against the results obtained from a set of experiments in which CVR is enacted upon a mobile phone charger, upon which varying amounts of supply voltage distortion are applied.

FORMULATIONS FOR NON-SINUSOIDAL POWER SYSTEMS BEHAVIOURS

Influence of Harmonic Current and Voltage Distortion on Apparent Power Injections

Prior to the introduction of some less renowned aspects of harmonic distortion, one should review the manner by which the non-fundamental portions of current and voltage, I_H and V_H, are distinguished from their fundamental counterparts, I_1 and V_1 [8]. The rms values for current and voltage are denoted in (3) and (4), as I and V. I_h and V_h correspond to the currents and voltages at the individual harmonic levels. THD_I is simply the ratio of I_H to I, while THD_V is the ratio of V_H to V.

$$I_H{}^2 = I^2 - I_1{}^2 \equiv I_{DC}{}^2 + \sum_{h=2}^{\infty} I_h{}^2 \tag{3}$$

$$V_H{}^2 = V^2 - V_1{}^2 \equiv V_{DC}{}^2 + \sum_{h=2}^{\infty} V_h{}^2 \tag{4}$$

At network nodes for which high levels of THD_I and/or THD_V are detected, the rms measurement for apparent power (S) may be observed to significantly exceed that of its fundamental constituent (S_1). An expression for Non-Fundamental Apparent Power (S_N) that encompasses the assortment of distortion and active powers existing at non-fundamental, harmonic frequencies is given in [8]. To derive accurate representations for apparent power under such conditions, S_N is defined in (5) as being orthogonal to the fundamental plane of active and reactive powers (P_1, Q). As such, the complete vector representation for S comprises three dimensions.

$$S_N = \sqrt{S^2 - S_1{}^2} \tag{5}$$

S_N is split into three separate terms in (6); Current Distortion Power (D_I), Voltage Distortion Power (D_V) and Harmonic Apparent Power (S_H), respectively [8].

$$S_N{}^2 = D_I{}^2 + D_V{}^2 + S_H{}^2 \tag{6}$$

Each of the D_I, D_V and S_H terms captures a different distortive coupling effect between the prevailing voltage and current signals at a network node of interest. These inter-relationships are expounded in Equations (7) to (9)

$$D_I = V_1 \cdot I_H = S_1 \cdot THD_I \tag{7}$$

$$D_V = V_H \cdot I_1 = S_1 \cdot THD_V \tag{8}$$

$$S_H = V_H \cdot I_H = S_1 \cdot THD_I \cdot THD_V \tag{9}$$

The dependency of each of the distortion power variables on different harmonic conditions is evident. For instance, (7) infers that D_I can only be non-zero if harmonic current distortion is present. Similarly, (8) shows that D_V can only be non-zero if some amount of voltage distortion exists, i.e. $THD_V > 0\%$. Finally, S_H can only arise if both forms of distortion exist (9). By substituting Equations (7), (8) and (9) into (6), expressions of S_N in terms of S_1 are formed in (10) and (11). It should also be noted that a similar derivation is presented in [14].

$$S_N{}^2 = S_1{}^2 \cdot \left[THD_I{}^2 + THD_V{}^2 + \left(THD_I{}^2 \cdot THD_V{}^2\right)\right] \tag{10}$$

$$\frac{S_N}{S_1} = \sqrt{\left[THD_I{}^2 + THD_V{}^2 + \left(THD_I{}^2 \cdot THD_V{}^2\right)\right]} \tag{11}$$

Linear Approximation for Non-Fundamental Apparent Power

Equations (3) to (9) demonstrate how varying degrees of supply and load distortion have the potential to significantly amplify the apparent power flows within affected networks. Moreover, the deliberations of [8] expose a potential shortcoming in the classic ZIP load modelling approach, within which the effects of current and voltage distortion are not typically considered. For implementations of CVR the ensuing disparity observed between modelled and measured fundamental and rms apparent powers may impinge upon network operators' ability to accurately assess how controlled adjustments to service-level voltages affect current flows and line losses.

The full impact of CVR on network conditions, across the harmonic spectrum, may be best evaluated via harmonic power flow based simulation. However, the accurate specification of ZIP load models for each harmonic order is time-consuming and may still not adequately capture the voltage dependency observed for the harmonic currents pertaining to certain device types. For instance, initial tests of modern luminaires in [10], show how a reduction in applied service voltage can elicit, in percentage terms, a parallel decline in associated harmonic current injections.

In light of the perceived inadequacies of the conventional ZIP load modelling approach, a linearized approximation to (11) is justified. Various quality of supply limitations conferred upon Distribution Network Operators (DNOs) render those THD_I ratios typically observed in practice to far exceed that of THD_V. Harmonic voltage characteristics for low voltage (LV) networks, as per Clause 4.2.5 of [13], stipulate for levels of THD_V observed at customer supply terminals to be less than 8 %. By contrast, the THD_I limits imposed upon Original Equipment Manufacturers (OEMs) in [11], for a myriad of appliances, are typically much less stringent. Indeed, for many loads rated below 25 W, no upper THD_I constraint applies [10]-[11].

Given the practicable ranges of THD_I and THD_V levels likely to be encountered, Figure 1 shows that the impact of harmonic disturbances upon apparent power flows and bus injections in LV networks is quantifiable by linear approximation. S_N/S_1 ratio values are determined via application of (11) and plotted in Figure 1 against possible THD_I conditions (between 0 and 250 %, in intervals of 50 %) for a selection of potential THD_V levels (between 0 and 8 %) that are consistent with statutory guidelines [13].

Owing to the narrow bounds applied for THD_V in Figure 1, its practical impact upon the S_N/S_1 ratio, when compared to that of THD_I, are observed to be negligible. On this theme [14] suggests that the same formulation used to represent D_I in (7) can be applied to approximate S_N with a 1 % degree of error. For completeness, the proposed linear approximation for S_N is repeated in (12).

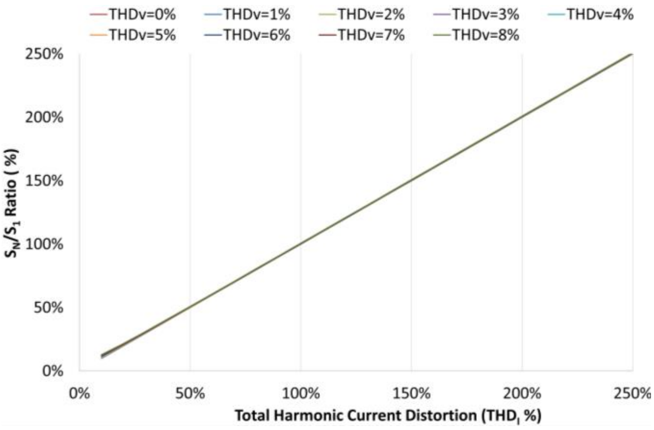

Figure 1: Apparent Power Ratio (S_N/S_1) vs Current Distortion, for different levels of Voltage Distortion

$$S_N \approx D_I \equiv S_1 \cdot THD_I \qquad (12)$$

If, for the sake of simplicity, THD_V is eliminated from the practical calculation of S_N, as per (12), and a ZIP load style approximation for THD_I can be validated, as inferred in [10] and presented for completeness in (13), then it ought to be possible for rms apparent power flows and bus injections to be resolved, to an acceptable level of accuracy, as functions of applied voltage alone.

$$THD_I(V) = THD_{I_0} \cdot \left[Z_{D_I} \cdot \left(\frac{V}{V_0}\right)^2 + I_{D_I} \cdot \left(\frac{V}{V_0}\right) + P_{D_I} \right] \qquad (13)$$

EXPERIMENTAL VALIDATION

The theory introduced in previous sections is now validated against a set of results obtained from testing the performance of a mobile phone charger, which is connected to a charging mobile phone. The device-under-test (DUT) converts the input AC supply voltage (rated between 100 and 240 V) to a 5 V rated DC output, in the form of a USB port. In each case the signal source used was a high precision, *Omicron CMC 256 plus* unit. Power quality metrics were measured using a *Fluke 435 PQ Analyzer*. The DUT was selected due to its evidently weak attenuation of harmonic currents, and the large values of S_N this coincides with. It therefore offers a vigorous test to the hypothesis discussed.

The DUT was tested at five different voltage set-points; 90 %, 95 %, 100 %, 105 % and 110 % of the nominal supply voltage level (230 V). Additionally, three different levels of THD_V were applied (0 %, 2.5 % and 5 %) for the aforementioned voltage magnitudes. The voltage spectra are scaled in proportion to a reference spectrum, produced to match the overall THD_V limit of 8% for LV networks, while adhering to the individual limits specified in Table 1 of [13]. The test conditions employed are presented in Table 1 for a supply voltage magnitude of 230 V. For each of the THD_V levels applied it is the rms voltage level that is maintained, not the magnitude of the fundamental.

Harmonic Order (h)	Test A	Test B	Test C	Reference Spectrum
THD_V	**0.0%**	**2.5%**	**5.0%**	**8.0%**
1	100%	99.97%	99.88%	-
3	0%	1.56%	3.13%	5.00%
5	0%	1.41%	2.81%	4.50%
7	0%	1.25%	2.50%	4.00%
9	0%	0.47%	0.94%	1.50%
11	0%	0.16%	0.31%	0.50%
13	0%	0.16%	0.31%	0.50%
$\|V_1\|$	**230.0 V**	**229.9 V**	**229.7 V**	-
$\|V\|$	**230 V**	**230 V**	**230 V**	-

Table 1: Laboratory Tests; Supply Voltage Conditions for a nominal rms voltage level (V) of 230 V

ZIP parameters for P and Q were determined from the results for each THD_V level and are shown in Table 2.

THD_V	P_0	Z_P	I_P	P_P	Q_0	Z_Q	I_Q	P_Q
0.0%	12.5	4.57	-10.1	6.54	1.50	28.6	-60.4	32.9
2.5%	9.00	6.34	-13.8	8.44	1.00	28.6	-59.1	31.5
5.0%	7.00	10.2	-21.1	11.9	0.50	28.5	-63.1	35.8

Table 2: Active and Reactive Power ZIP Coefficients observed at different levels of THD_V

Similarly, ZIP coefficients for THD_I, as per (13), were determined. These are presented for Test A only in Table 3, in which no voltage distortion is applied, so that the potential coupling of current and voltage harmonics, expressed in the definition for S_H in (9), is avoided.

THD_V	THD_{I0}	Z_{DI}	I_{DI}	P_{DI}
0.0%	241 %	-0.90	2.52	-0.63

Table 3: ZIP Coefficients for THD_I

For other literature in which ZIP coefficients for P and Q are measured, the impact of THD_V on the results is not explicitly considered. Additionally, the effects of THD_I on apparent power are not discussed [5], [9]. As such, the values estimated for S under the conventional ZIP method, and which are depicted in Figure 2, Figure 3 and Figure 4 (Method I, blue trend), are determined using the P and Q coefficients measured at each of the respective THD_V levels (listed in Table 2).

The results documented for Method II in the same charts (red trend) are calculated from the ZIP coefficients found for the THD_V = 0% case in Table 2, from which S_1 is determined. THD_I is then estimated from the prevailing voltage level, as per (13) and using the ZIP coefficients set out in Table 3. From this S_N is estimated via (12). Finally, S is calculated via the rearrangement of (5).

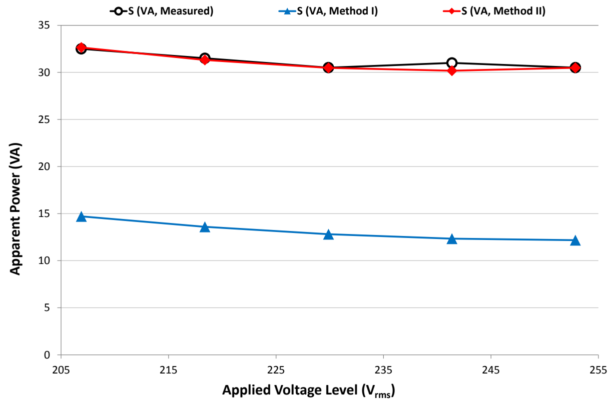

Figure 2: Measured and Estimated Apparent Power vs Applied Voltage (Test A, THD_V = 0.0 %)

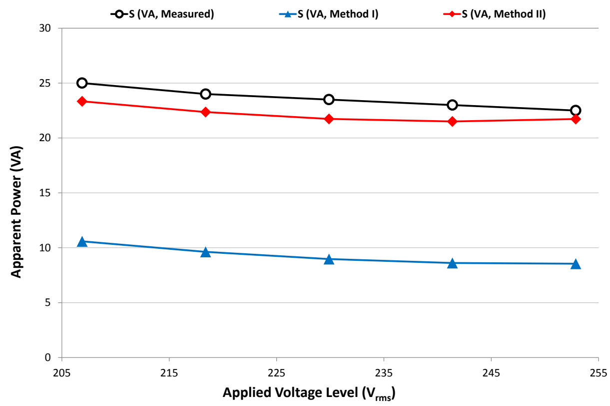

Figure 3: Measured and Estimated Apparent Power vs Applied Voltage (Test B, THD_V = 2.5 %)

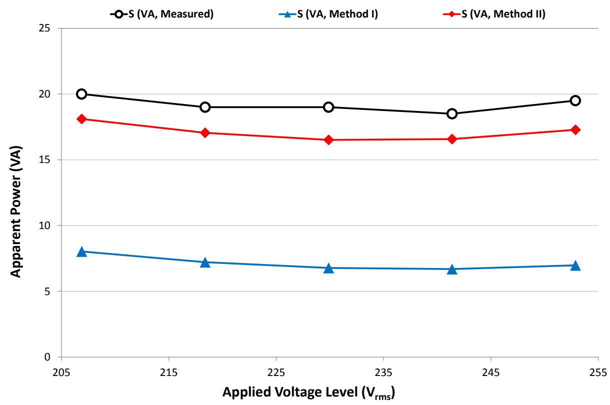

Figure 4: Measured and Estimated Apparent Power vs Applied Voltage (Test C, THD_V = 5.0 %)

DISCUSSION AND CONCLUSIONS

This paper proposes a means by which the effectiveness of CVR in reducing technical losses can be better quantified in the presence of harmonic current and voltage distortion. It is argued that the classic approach to ZIP load modelling can be extended to incorporate a metric for THD_I which, as [10] postulates, may be modelled as a function of applied voltage in a similar manner to that of P and Q.

Various definitions for distortion powers, documented in IEEE 1459-2010 [8], are introduced as a prelude to the contention that an approximation for flows and injections of Non-Fundamental Apparent Power (S_N) in LV networks can be reliably formed from an expression for Current Distortion Power (D_I). This holds true so long as the prevailing level of THD_V remains within limits [13]. From the new load model configured for THD_I, and the equations highlighted from [8], the rms Apparent Power (S) may be determined. This in turn may be used to calculate how rms current flows are affected by changes to voltage levels at load buses.

The accuracy of the linear approximation for S_N is corroborated against practical experimental results for a low powered, harmonic current polluting device (a mobile phone charger). The results depicted in Figure 2 show that the approximation is robust for conditions in which high levels of THD_I apply but no THD_V is present (an average, relative error of 1.2 % is observed). As higher levels of THD_V are applied the accuracy of the approximation declines, such that a worst case, average, relative error of 11.0 % is recorded for Test C. This is consistent with the expectations set out in [14]. However, in both Figure 3 and Figure 4 the values estimated for S are much closer to the measured quantity than those determined via the classical approach, in which only those ZIP models outlined in Equations (1) and (2) are utilised and for which a worst case, average, relative error of 62.9 % is shown for Test C.

The updated approach to ZIP load modelling advocated by this paper has been successfully validated against a set of practical laboratory results. These results suggest that the experimental determination of ZIP models for P and Q should take into account the harmonic distortion that is present in the applied voltage during testing. Moreover, to obtain the most accurate voltage-response characteristic of the loads under test, and so better reflect their real world operation, ZIP parameters should be determined whilst THD_V is applied at its minimum level. Additionally, ZIP models that express the harmonic current distortion attributed to a load can prove to be a useful analytical supplement when modelling the effects of voltage variations in networks for which high levels of harmonic pollution exist. This evaluation is specifically pertinent to the ever growing penetration of constant power load types within LV networks. Devices of this nature inherently contribute to emissions of non-fundamental currents and powers and their associated technical losses.

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