THD MINIMIZATION OF MULTILEVEL INVERTER WITH OPTIMIZED BOTH DC SOURCES MAGNITUDE AND SWITCHING ANGLES

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ABSTRACT

Multilevel inverter is a power electronic device that has many attractive features like high voltage capability and near sinusoidal output making them suitable for high power applications. On the other hand harmonic distortion from the modern switching mode power converters has become a serious problem in utility. Total Harmonic Distortion (THD) minimization is a complex problem with multiple minima. Various THD minimization methods have been proposed in papers that just optimize the switching angles of the multilevel inverter. In this paper both DC input sources magnitude and switching angles are optimized with Particle Swarm Optimization (PSO) algorithm to minimize the THD of the output staircase voltage of the multilevel inverter. The impact of the proposed minimization method on voltage magnitude optimization and increased number of switching angles optimization on the staircase output voltage is analyzed. The effectiveness of the proposed method is validated by simulation results of a 7level inverter. The proposed method's THD, output voltage level and number of the switching angles is compared with other techniques and influence of the input dc sources optimization on the THD minimization is shown.

INTRODUCTION

Nowadays capability of multilevel inverter operation on high voltage and powers and generating high quality voltage waveforms receives more and more attentions. Multilevel inverters generate the desire staircase voltage waveform in the output with suitable summation of input dc sources. By increasing the number of input dc sources the available DC levels increases and therefore the quality of the output voltage can be increased. Most of the multilevel inverters are divided in to three well known types which are: cascaded H-bridge multilevel inverter (CHB), flying capacitor multilevel inverter (FC) and neutral point clamed multilevel inverter (NPC). While these are the basic types of multilevel inverters recently a variety of modified multilevel inverters have been proposed in the papers [2-7]. In the reference [8] we have proposed symmetric and asymmetric multilevel inverter that uses reduced number of power switches in its structure. Output voltage of the multilevel inverter is composed of several dc sources.

Various control strategies such as different types of pulse width modulation (PWM) and space vector modulation (SVM) have been suggested in the papers in order to decrease the undesired harmonics from the output waveforms of the multilevel inverters. The main problem of these techniques is their inability to completely eliminating the low-order harmonics. Selective harmonic elimination methods have been suggested in the papers that adjust switching angles in order to eliminate specific harmonic from the output of the multilevel inverter [9-14]. The main problem with this method is the difficulty of obtain unique answer from polynomial equations.

Numerical iterative techniques such as Newton-Raphson can solve the problem in some conditions but they needs suitable initial guess that should be around the exact answer. Providing such guess is difficult in most cases.

Most recent control strategies of multilevel inverter are artificial intelligence methods such as genetic algorithm (GA) and particle swarm optimization (PSO)[15,16]. With increasing the number of switching angles these methods may trap in to various local optimum points. So, appropriate adjustment of the algorithm operators is necessary to achieve optimized answer. Nowadays different methods have been proposed to minimize the total harmonic distortion (THD) of output voltage in multilevel inverters [9-16]. These methods minimize all harmonics including triples. In [1] a Species based PSO has been proposed in order to minimize THD of multilevel inverter in which the number of switching angles have been increased so that in each output level the voltage varies between previous and present levels. So, the fundamental component of the output voltage will be more sinusoidal which means lower THD.

In this paper in addition to increasing the number of switching angles in each level that have been done in other works [9-16], the voltage magnitude input of dc voltages of the multilevel inverter are optimized with PSO algorithm too. These suggestions have resulted in significantly decreasing of THD of the output voltage without increasing the switching losses. The rest of this paper is organized as follows: in section II a multilevel inverter with reduced number of power switches have been proposed. In section III the proposed method of THD optimization in multilevel inverter have been investigated. In section IV the employed PSO algorithm, its fitness function and particle selection have been analyzed. Finally simulation results and conclusion have been presented in sections V and VI respectively.

MULTILEVEL INVERTER WITH REDUCED NUMBER OF POWER SWITCHES

A single phase schematic diagram of a 7level inverter is shown in Fig. 1. As it can be seen in this figure the inverter has 10 power switches in its structure. The inverter is composed of two parts which are: level generator part and H-bridge part with 6 and 4 power switches respectively.

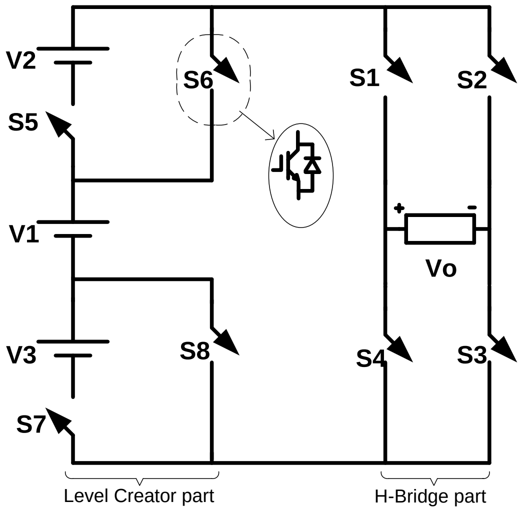

Fig. 1 7 level inverter

Level generator part uses specific arrangement of input dc sources to create output voltage levels. The H-bridge part changes the polarity of the output voltage in each half cycle. The dc sources have been separated with each other by a series power switches and can be bypassed by another parallel power switch [8]. In order to have a 2n+1level inverter n dc sources would be required that should be equipped with 2n+2 power switches. The amplitude of the dc sources can be different. The dc sources and switching angles can be optimized with PSO algorithm in order to minimize the THD. The case study of this paper is a 7level multilevel inverter and the proposed algorithm can be used for any type of multilevel inverters with different voltage sources and switching angles that must be optimized. As it can be seen in the Fig. 1 for a 7level inverter 3voltage sources with 8 switches is needed.

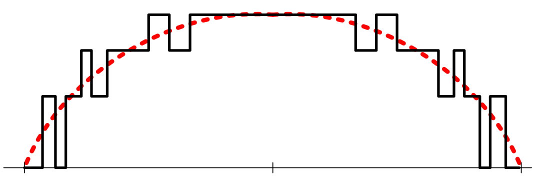

Fig.2 Staircase voltage with variable dc link voltage and increased switching angles

PROPOSED THD MINIMIZATION METHOD

Multilevel inverters generate staircase voltage waveform in the output which still contains different harmonics. Different methods have been suggested to decrease these harmonics [9-20]. For minimizing the THD it’s necessary to adjust the switching angles and voltage magnitude of dc sources in such a way that the output voltage be as sinusoidal as possible. For this purpose, the number of the switching angles has been increased and as it can be seen in Fig. 2, in each output level the voltage changes between current and previous voltage level [17]. By using this switching strategy in addition to pulse width modulation in each voltage level it is possible to have a significant decrease in THD. However, as multilevel inverters are used in high and medium voltage levels, the switching frequency is limited. With excessive increase in the number of switching angles the switching losses of the multilevel inverter will increase. So, in order to prevent excessive increase in power losses, the input dc sources voltage magnitude of the inverter can be optimized. By optimizing the dc voltages and the switching angle’s it is reasonable to expect an optimized output staircase voltage with minimum THD and reduced switching losses.

The main goal of this paper is to optimize the THD of the staircase output voltage with appropriate selecting of switching angles and dc voltage sources. The THD of the output voltage for nontriple harmonics can be calculated from following equation [21].

$$THD = \frac{\sqrt{\sum_{n=5,7,11}^{49} V_n^2}}{V_1} \tag{1}$$

In this equation n is the number of the output voltage harmonics, V_1 is the fundamental harmonic component of the output voltage and V_n is the amplitude of nth harmonic of the output voltage. It should be noted that the triple harmonics be eliminated in three phase systems and as the output voltage is symmetric, the even order harmonics do not exist.

PARTICLE SWARM OPTIMIZATION ALGORITHM

Kemely and Eberhart were the first persons that introduce Particle swarm optimization algorithm as an intelligence optimization algorithm in 1995[22]. As this algorithm inspired by the birds and ants livings sometimes called as ant colony algorithm or bird’s flock algorithm. However PSO is population based algorithm that each person of the population is like a particle of the swarm. Each particle is an answer for optimization problem. Each particle updates its position in the swarm from its history of own best position and best position of the other particles in every iteration. Position measurement of the particles depends on their fatnesses in the fitness function. As a result each particle that has better answer for optimization function introduced as a better position.

In the first stage initial population of the particles generated. Different solutions have been suggested to the initial population generation. With proper selecting of the initial population the algorithm's speed increases but it may trap to a local minimum. It's necessary to have vast generation for initial population to avoid the local minimums. Each particle of the swarm composed of different components that are the problem's variables. Each variable has a particular limit that should be applied.

In the second stage the generated population's fitness should be calculated. Among the whole particles of the population during the iterations, the particle with the best fitness selected as the global best that is known as gbest. Each particle updates its position with a velocity that depends on the particles history for its best positions that is known as P_{best} and the whole population's best position.

$$X_i = [X_{i1}, X_{i2}, ..., X_{iD}] \quad (2)$$

$$V_i = [V_{i1}, V_{i2}, ..., V_{iD}] \quad (3)$$

$$P_{besti} = [P_{bi1}, P_{bi2}, ..., P_{biD}] \quad (4)$$

$$g_{best} = [g_{b1}, g_{b2}, ..., g_{bD}] \quad (5)$$

$$V_{id}(t+1) = \omega(t)V_{id}(t) + C_1 r_1 (P_{id} - X_{id}(t)) + C_2 r_2 (g_{bd} - X_{id}(t)) \quad (6)$$

$$X_i(t+1) = X_{id}(t) + V_{id}(t+1) \quad (7)$$

In these equations X_i is the position vector for ith particle, V_i is velocity vector for ith particle, P_{besti} is the best position of the ith particle during iterations, g_{best} is the best position of the particles among the whole population during the iterations, D is the number of components of each particle, C_1 and C_2 are the cogitative and social parameters respectively, r_1 and r_2 are random values between [0,1] and $\omega(t)$ is convergence factor of tth iteration. In order to increase the optimization speed and avoid trapping in the local minimum it is necessary to select a proper convergence factor:

$$\omega(t) = 1 - \frac{t}{t_{\max}} \quad (8)$$

Where t is the current iteration's number and t_{max} is the maximum number of the iterations will be done. The fitness function for THD optimization problem can be written as follow:

$$Fitness\ \ Function : \{5 \times |V_1^* - V_1| + THD\} \quad (9)$$

In this equation THD is the total harmonic distortion of the output staircase voltage, V_1 is real value and V_1^* is the reference value of the fundamental component of the output voltage respectively. In order to have exact value of fundamental component in the output of the multilevel inverter the error of the reference value and real value is multiplied in 5. The limitations for switching angles and dc voltages are as follows that should be applied in the particles in every iteration.

$$\begin{aligned} &for \quad i = 1, 2, ..., 3m-1 \qquad \alpha_i \le \alpha_{i+1} \le \pi/2 \\ &for \quad j = 1, 2, ..., m-1 \qquad v_j < v_{j+1} \end{aligned} \quad (10)$$

Where m is the number of input dc sources, α_i is the ith switching angel and v_j is the jth dc voltage source. In the proposed optimization algorithm for multilevel inverter with m dc sources the output voltage has 2m+1 level and there are 3m switching angles in each quarter.

SIMULATION RESULTS

The 7level inverter indicated in Fig.1 have been simulated in MATLAB SIMULINK software and voltage amplitude of dc sources and switching angles have been optimized with PSO algorithm. The simulation results for output staircase voltage against sinusoidal voltage is shown in Fig.3. the THD of the output voltage have been minimized down to 3 percent. On the other hand increasing number of switching angles per each level leads to better THD but increases the power switching losses. So in order to prevent increasing of these losses the switching angles limited to 3angles per each level.

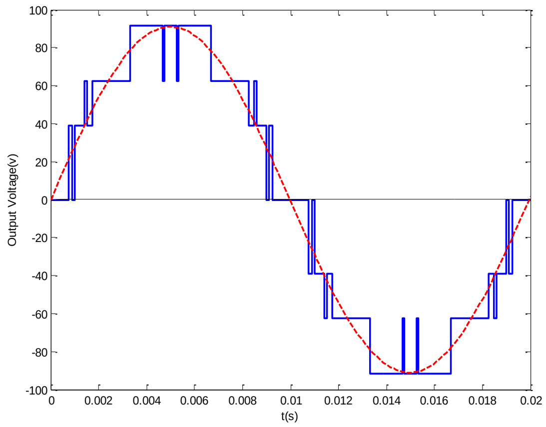

Fig.3 Multilevel inverter output staircase voltage and sinusoidal waveform.

As it can be seen in the Fig.3 the dc voltage levels are different and have been optimized to reduce the output THD(table I). In table II some of the first harmonic orders of the output staircase voltage have been shown and A comparison of the proposed method and other THD minimization methods has been illustrated in table III.

Table I. Optimized voltage magnitudes

Input dc voltage source	Optimized magnitude
V_1	39.05 v
V_2	23.33 v
V_3	29.07

Table II. Harmonic orders

Harmonic order	Optimized magnitude
5	0.3%
7	0.6%
11	0.91%
13	0.09%
17	1%
19	0.95%
23	0.77%
25	0.59%

Table III. Comparison of THD

Method	Number of output voltage level	Number of switching angles per quarter	THD
The perposed method	7	9	3.78
[23]	13	6	4.33
[24]	11	20	5
[25]	7	More than 50	2,78
[26]	9	More than 50	10

As it can be seen in this table the proposed method has the best THD due to lower number of switching angles per quarter of cycle. In fact our multilevel inverter shown in Fig.1 uses the minimum number of power switches and by using of the proposed control method for THD minimization the inverter can be a economical multilevel inverter that has reduced number of power switches and the best THD according to lower switching power losses.

CONCLUSIONS

In this paper an optimization method with variable dc sources and increased switching angles for minimizing the THD of the output voltage of multilevel inverters have been proposed. In this method output staircase voltage of multilevel inverters minimizes with optimization of both magnitude and switching angles of the inverter. As it can be seen in simulation results the proposed method has been examined on 7level inverter and its THD has been minimized. In comparison with other methods that have been proposed in papers according to number of switching angles and the switching losses the proposed method of this paper has a better THD.

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