SETTING AND ALGORITHM SIMULATION OF PV ANTI-ISLANDING PROTECTION IN CASE OF INCREASED FREQUENCY THRESHOLD

Budi SANTOSO
PT PLN (Persero) – Indonesia
budis54n@pln.co.id

Bertrand RAISON
G2E Laboratory – France
bertrand.raison@g2elab.grenoble-inp.fr

Ngapuli SINISUKA
ITB Bandung - Indonesia
ngapuli@hv.ee.itb.ac.id

ABSTRACT
UOVR and UOFR as passive anti-islanding methods lack of sensitivity to detect islanding. The performance gets worse when the frequency threshold is increased from 50.2 Hz to 50.6 Hz. For instance, dedicated passive methods such as ROCOF help the inverter to detect islanding. When active methods such as SFS and SVS are activated, the number of detected islandings is increased to 87.5%. To improve the number of detected islanding and to reduce the number of false trippings, an under voltage blocking scheme and zero crossing detection are implemented. As results, the inverter could detect 100% of islanding event with 13.3% of false tripping. As future work to reduce the number of false tripping, a study implementing impedance measurement with a closed loop simulation could be done.

INTRODUCTION
DIN VDE 0126 is one of the standards used as guidance to implement anti-islanding protection. It covers three major protection algorithms: under/over voltage, under/over frequency, and islanding detection. DIN VDE 0126 has changed by increasing the frequency threshold to 47.5-50.2 by 2006 [1]. In the middle of 2014, France has increased its frequency threshold to 47.5-50.6 Hz.

The research is conducted by doing simulations using power system simulation software EUROSTAG to obtain the system behavior under several events such as line opening, loss of generation, and fault. The output of the simulation, voltage and frequency, is then used to generate voltage as input for low voltage simulation (including PV and anti-islanding algorithms). The result of these latest simulations is then analyzed to have an understanding of the following matters: the effect of the increased acceptable frequency threshold to the performance of anti-islanding protection, the possibility to improve anti-islanding performance by implementing new protection scheme and or setting, and the possibility of active method implementation in addition to passive method.

MODELLING
To perform the study, a complete network model needs to be built. Electrical network model consists of three main parts: high voltage (HV) level of transmission system (400 kV), medium voltage (MV) level of distribution system (20 kV), and low voltage (LV) level of distribution network (400 V) where the PV is connected at its point of common coupling (PCC). Both HV and MV network models are built using EUROSTAG software. While the LV network, inverter control, measurement block, and protection block are modeled using Matlab Simulink.

The load connected to PV when islanding occurs is a parallel RLC load (R=16.6Ω, L=16.79mH, C= 604mF).

Voltage and Frequency Measurement
Voltage measurement is done by using simulink rms voltage measurement block. Frequency and its rate of change are measured by using the output of PLL. The other method used in this simulation to measure frequency and its rate of change is zero crossing detection (ZCD). ZCD measures frequency by detecting the time when the voltage value crossing the zero line from its positive value to negative value and vice versa. By knowing those points, calculation of frequency can be made.

Under and Over Voltage Protection
The model of under/over voltage relay (UOVR) is built by using rms voltage as input to the block. Tripping command will be issued if the rms voltage is outside the allowable voltage band for a particular time longer than the determined time delay. Separated under voltage block
is used to makes the signal independent from the block designed for UOVR protection. The block is not connected to time delay block, so when the rms voltage sensed below the setting value, blocking signal will be sent to UOFR and ROCOF immediately.

**Under and Over Frequency Protection**
When the frequency is outside the threshold (it is lower than under frequency limit or higher than over frequency limit) for more than the time delay, a tripping command will be issued. It is connected to time delay block to make sure that it will only trip when islanding occurs. IEEE std 1547-2003 specifies 0.16s for UOFR time delay, while DIN VDE 0126 (February 2006) specifies 0.2s as UOFR maximum time delay. A value of 0.12s is chosen as time delay implemented on this model, as it comply the requirement stated on the both standards.

**Rate of Change of Frequency Protection (ROCOF)**
The value of rate of change of frequency commonly used as setting value varies in the range $0.1\text{Hz/s} - 1.2\text{Hz/s}$ with time delay adjustable from 0 to 700ms [3]. There is also an effort to use analytic formula to determine this setting by taking power unbalance, required time detection and system inertia into account when calculating it[4]. For this simulation, the setting of ROCOF is $0.125\text{Hz/s} - 0.25\text{Hz/s}$ and 0.12s for its rate of change and time delay setting. This setting met also the minimum suggestion provided by [5].

**Sandia Frequency Shift (SFS)**
The basic principle of SFS is an accelerated frequency drip with positive feedback. In the presence of grid, the frequency will not be drifted; on the contrary when the grid is missing the frequency will drift [6].

SFS is implemented through the concept of zero current segment to create accelerated frequency drift based on the measured voltage. This zero current segment is also expressed as chopping factor which represent the ratio between the length of zero segment to the length of a half cycle. SFS block diagram is designed to be able to control the output current of the inverter according to the implemented chopping factor. Performance of SFS is controlled by the setting of its frequency difference gain (KSFS). By choosing KSFS= 3, the THD of the current is equal to 1.53% and this chosen setting value could help detecting islanding event quickly as reported by [2].

**Sandia Voltage Shift (SVS)**
SVS gain, Ksvs, is chosen so that it does not cause power deviation more than 5% under normal condition. By choosing Ksvs equal to 0.1 and assuming that the maximum allowable voltage deviation is 10% lower of the rated voltage, it will cause the current output lower by 1%.

**SIMULATION AND RESULTS**

**Case Selection**
Simulation cases are selected to represent various events that could happen in HV, MV, and LV network. The cases are selected to have the system behavior under faulty condition (both steady state and temporary fault), intended line opening, loss of generation unit, and loss of load. All the cases are considered to have worst effect to anti islanding detection. There are 23 cases obtained to represent these conditions. Additional cases are introduced to validate and observe the stability and sensitivity of anti-islanding protection when the load parameter is modified. The parameter is modified as listed on table 1.
**Protection Model**

This study will use several protection models. The complete models used in this study can be seen on table 2.

<table>
<thead>
<tr>
<th>Case</th>
<th>Inductance</th>
<th>Capacitance</th>
<th>Case</th>
<th>Inductance</th>
<th>Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>L+1%</td>
<td>C</td>
<td>29</td>
<td>L+5%</td>
<td>C</td>
</tr>
<tr>
<td>25</td>
<td>L+5%</td>
<td>C</td>
<td>30</td>
<td>L+10%</td>
<td>C</td>
</tr>
<tr>
<td>26</td>
<td>L-5%</td>
<td>C</td>
<td>31</td>
<td>L-10%</td>
<td>C</td>
</tr>
<tr>
<td>27</td>
<td>L-5%</td>
<td>C</td>
<td>32</td>
<td>L-10%</td>
<td>C</td>
</tr>
<tr>
<td>28</td>
<td>L+5%</td>
<td>C</td>
<td>33</td>
<td>L+10%</td>
<td>C</td>
</tr>
</tbody>
</table>

**Table 1. Additional case with varying LC parameter**

**Simulation Result and Analysis**

The performance of each protection model is evaluated by scoring the ratio between the number of false operations and total events for islanding events, HV events, and MV events. The performance judgment of anti-islanding is done by plotting the scores on three axes. The smaller area covered by triangle the better performance of the protection. Percentage of protection performance is also manifested on 2 terms. First, the ratio of the number of cases detected and the total number of islanding cases. Second, the ratio between the number of false tripping and the number of cases which the inverter should not detect.

**Protection Performance Observation on Existing Setting**

The existing protection is represented by model 1 and 5 on Table 2 (with deactivated ROCOF), which has PLL and ZCD based frequency measurement respectively. The UOVR and UOFR performance of model 1 and model 5, as depicted by Figure 5, shows that the existing protection device and setting tend to fail to work properly, moreover in detecting islanding. On model no.1, UOVR and UOFR fail to detect all of the islanding events and produce 13.33% of false tripping. While on model no.5, UOVR has 0% performance in detecting islanding and 13.33% of false tripping command, and UOFR has 0% both in detecting islanding and percentage of false tripping.

**Protection Performance Observation on New Frequency Setting**

The implementation of new frequency settings is represented by model 2 and 6. As the only change made is upper frequency threshold setting, the performance of UOVR is remain unaffected. It is already known on the previous simulation that the performance of anti-islanding which relies only on UOVR and UOFR has a low performance. The increase of upper frequency threshold reduces the protection sensitivity to detect islanding, but it also means that it could reduce the number of undesired tripping as can be seen on Figure 6. The performance is better when the fault in on HV side, but it needs to be confirmed whether it has the same performance in case islanding event. The result of additional islanding tests is depicted on Figure 7. It shows that the increase of the frequency threshold will cause the number of undetected events of islanding to increase.

**Application of ROCOF**

Figure 8 shows that ROCOF is able to detect more islanding events than those detected by UOFR. It also offers a faster detection time compared to UOFR. Since ROCOF is not affected by the increasing value of upper frequency threshold, the performance is remaining the same even though the UOFR setting has been changed in model no.2.
Application of SFS and SVS
Model no. 3 is suitable to represent anti-islanding protection with SFS and SVS enabled. Observation on islanding event can be seen on Figure 9. The frequency and its rate of change measured by the model are greater than those measured by models whose SFS is inactivated. The figure shows that models with SFS and SVS activated have very important frequency difference which is very valuable in making the islanding detection become faster and easier.

By using model no.3, detection time of islanding event is improved as well as the number of detected events. For case 1 to 23 used in the simulation, the detected islanding cases by UOFR are 75%, while the number of false trippings is 20%. ROCOF has 87.5% and 33.3% for its number of detected islandings and number of false trippings respectively. SFS and SVS make the protection successfully detect almost all of islanding events; this performance is depicted by Figure 10 and 11.

Application of Under Voltage Blocking
Model no. 4 represents an anti-islanding protection with its UOFR and ROCOF connected with under voltage blocking signal. It has a better performance compared to the one without under voltage blocking (model no. 3). There are improvements on its performance in dealing with HV events; this makes the area covered by the triangle on Figure 12 become smaller (both for UOFR and ROCOF) compared to previous cases.

The ability of protection model no. 1 to 4 to detect islanding and the percentage of false trippings are summarized on Table 3. The Table shows that model no. 4 is the best model so far: it uses the combination of ROCOF, SFS, SVS, and under voltage blocking. But it is still not able to completely eliminate the false operation of the protection.

Performance of ZCD Frequency Based Protection
The performance of model no. 5 to 10 is depicted on Figure 13. By observing the figure, it is obvious that with SFS and SVS activated and ZCD based frequency measurement, the UOFR of model no. 9 and 10 have the best performance among the others. ROCOF of model no. 10 has the best performance among the others.

Model no. 10 also shows its superiority when it is compared to model no. 1 to 4 (Figure 14). Time detection of islanding is also impressive compared to the other model. Figure 15 shows the time detection performance of model 10: it is the fastest one. Simulation results show that the use of ZCD, SFS, SVS, and under blocking as it is implemented on model no.10 gives a good performance (100% islanding detected, 13.3% false tripping). UOFR cannot detect 2 cases of the provided islanding cases, while ROCOF is able to detect all the
islanding cases. Model no. 10 is too sensitive in detecting fault which happens at the other MV feeders close to 20 kV bus.

The less area covered, the better its performance.

**Determination of the Most Suitable Protection Model Dealing with Grid Code Change**

The suitable model to be used for LV application when grid code frequency thresholds are changed should ideally have the ability to detect all of the islanding cases and remains unaffected for events that happen on HV and MV network. To find the most suitable model, all of the 10 models are being compared based on the minimum number false operations for events at HV, MV, and islanding cases. It is expressed by the area of the triangle. The less area covered, the better its performance.

The performance of UOVR and UOFR are depicted by figure 16. It shows that model no. 9 and 10 has the best performance for its UOVR. The best performance of ROCOF belongs to model 10. The performance of ROCOF can be seen on figure 17. Figure 18 shows the total area covered by triangle. And the best suitable model with the smallest area is model no. 10.

**CONCLUSION**

This work shows that the passive method anti-islanding with conventional under/over voltage (UOV) and under/over frequency (UOF) protection have a lower performance when the frequency threshold is increased. The implementation of SFS and SFS helps the protection to achieve a better anti-islanding performance compared to the passive method. The implementation of ZCD as a mean to measure the frequency is proved giving the best performance of the anti-islanding with SFS and SVS activated, but it still has the possibility to send false tripping command especially when the fault occurs near point of common coupling of the PV.

**ACKNOWLEDGMENTS**

The authors would like to acknowledge the contribution of Julien BRUSCHI for providing the LV network model and inverter control model used in this work.

**REFERENCES**


