VOLTAGE FLICKER REDUCTION WITH SVC IN STEEL PLANT

Zhongyuan ZHAO
NR Electric Com., Ltd. – China
zhaozy@nrec.com

Feng XU
NR Electric Com., Ltd. – China
xuf1@nrec.com

Ke LI
NR Electric Com., Ltd. – China
lik1@nrec.com

ABSTRACT

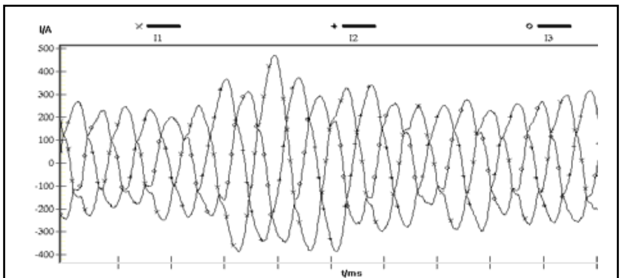
The voltage flicker is main factor influencing the power quality and SVC is well-proven solution. The flicker reduction requires very short response time, according to the relation analysis between flicker improvement factor and response time. SVC has a fast open-loop control function to achieve effective voltage support. The fast algorithm of flicker reduction is presented here based on synchronization sequence decomposition and phase-locked, which makes it strong immunity to serious power environment. Filter parameters are optimized with good harmonic suppression function. Step response and site performance test are performed to show that this algorithm can get rapid response and better improvement of flicker reduction about 50%. This flicker reduction controller is enough effective and available in industrial application and makes good economic benefits.

INTRODUCTION

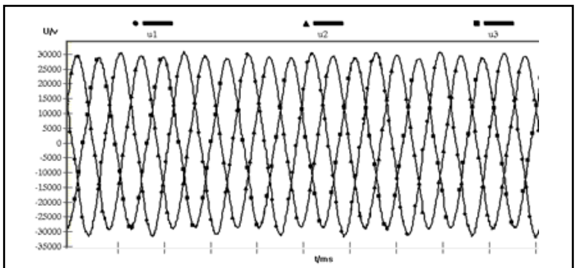
With increasing electricity load and its consumption, especially the impact of power load causes serious pollution of the power quality in the power distribution system [1]-[3]. This not only affects the quality of local power supply, and also influences nearby supply through power network coupling.

Electric arc furnace is one of typical impact loads, which always brings non-period and asymmetrical short-circuit case. It is a complex and heavy load and is a large, unbalanced, and strongly fluctuating consumer of reactive power. These reactive power fluctuations which are very marked, especially at the beginning of the melting operation, lead to voltage drops and fluctuations that reduce the active power to the arc furnace and also to other loads connected to the same feeding bus bar.

These results cause serious voltage fluctuation and flicker problem. The on-site measuring voltage and current curve of 30 ton EAF in operation is shown in the figure 1.



a. current curve



b.voltage curve

Figure 1. Voltage and current measurment curve of EAF load

THE MECHANICS OF SVCS

SVCs traditionally comprise a combination of breaker switched Fixed Capacitor Banks that provide the capacitive reactive power and Thyristor Controlled Reactors (TCR) that provide the dynamically controlled inductive reactive power.

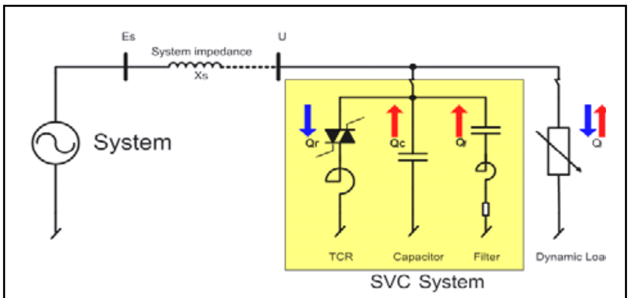


Figure 2. Typical Configuration for SVC System.

By controlling the firing angle on the thyristors, the current flowing in the TCR is rapidly controlled. The thyristors are very fast acting, which means that the reactive power output of the TCR can be changed in less than a cycle.

A downside of the operation of the thyristors is the introduction of harmonic currents into the system. The fixed capacitors are designed to absorb the harmonic currents. Thus the SVC does not introduce unacceptable harmonic levels into the network.

The rapid respond of SVC system makes the industrial grid achieve the good performance in operation. So SVC compensation device in the power supply system is indispensable and very important. Reasonable choice and design, configuration, must be implemented to minimize the network loss, to improve the quality of the grid.

FLICKER REDUCTION METHOD

Until now, the effective way in the global to reduce this kind of voltage flicker has been to install dynamic reactive power compensation. Dynamic reactive power compensation has very short response time so as to follow the real-time demand of load, which makes the impact influence become small to the power supply and then get better power quality. Static Var Compensator (SVC) is widely used in metallurgy industry to solve this problem.

The principle is with the real-time monitoring of the SVC control system, to calculate the control objectives. According to the dynamic load changes and power system requirements, automatically switch filter capacitor bank, and dynamic continuously to adjust TCR inductive reactive output.

The flicker improvement is mostly depend on the response time of SVC control. The corresponding relation among flicker improvement factor, control response time and reactive power compensation degree is shown in figure 3.

The flicker improvement factor is defined as the formula below.

$$(Pst_0 - Pst)/Pst_0 * 100 \tag{1}$$

where Pst_0 is the flicker value before improvement, Pst is the flicker value after improvement.

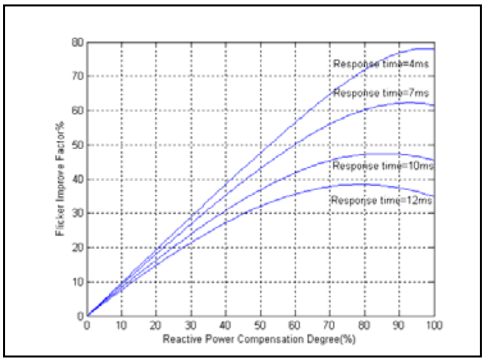


Figure 3. Relation between flicker improvement and control response time.

The figure 3 shows that shorter response time makes higher flicker improvement factor. If the flicker improvement factor wants to be more than fifty percent, the control response time of SVC shall be required to less than 9.5 milliseconds. In engineering, many SVC supplier can only provide the flicker improvement factor of thirty percent. It is very important to increase economic benefits with high flicker improvement factor.

Flicker Reduction Algorithm

Firstly, this paper presents synchronization coordination phase-lock method based on sequence component. This method transforms the positive sequence and negative sequence in synchronization coordination system, and locks the phase angle of positive sequence component of fundamental power frequency. This method is simply and effective, so as to eliminate the error caused by the traditional synchronization phase-lock method.

In this method, the phase information of three-phase voltage（u_a, u_b, u_c） can be obtained by transforming three phase voltage into two phase voltage（u_α, u_β）, and then transforming the two phase voltage into （u_d, u_q）in synchronization rotation coordination system. In this way, the phase angle θ can be got by following the voltage space vector $Ue^{j\omega t}$. Assuming the voltage space vector is same as the d axis's vector, the phase angle is calculated as $\theta = \omega t$.

The voltage vector in synchronization coordination system can be express as flows.

$$\begin{aligned} U_d &= \frac{3}{2}U_m \cos(\theta - \theta^{'}) \\ U_q &= -\frac{3}{2}U_m \sin(\theta - \theta^{'}) \end{aligned} \tag{2}$$

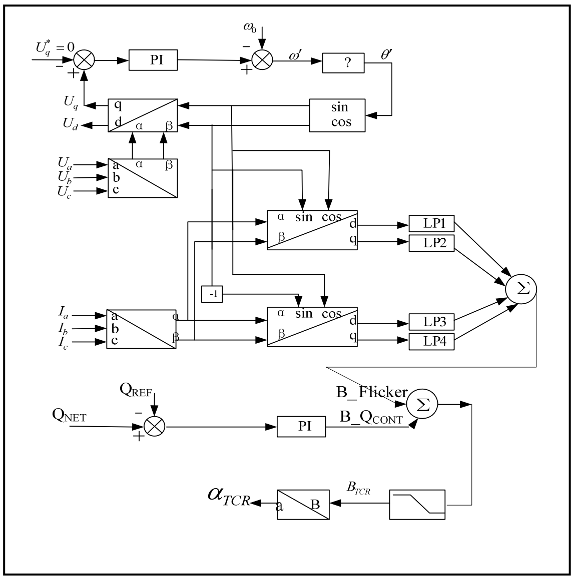


Figure 4. Function block of voltage flicker reduction algorithm.

In phase locking process, the phase difference $\Delta\theta$ between input voltage phase θ and phase tracing angle $\theta^{'}$ is calculated in real time. This difference shall be equal to zero by PI regulator in engineering practice. Then output phase angle of phase-locked loop can be taken as the phase angle of voltage in fundamental power frequency for phase A.

According to the synchronization phase-locked angle and

frequency, the load current can be decomposed in sequence component in interruption time of one hundred microseconds, and then component in both d axis and q axis for positive and negative quantity can be achieved as in figure 4.
Low pass filter is also key part in this process. Its parameters shall be obtained by optimization.

$$LP(s) = \frac{Kp}{1 + sTi} \qquad (3)$$

Where Kp is proportional coefficient , Ti is time coefficient, $s = j\omega$, ω is angular frequency.

The susceptance of voltage flicker reduction can be achieved by current sequence component analysis. This susceptance is added with the one required by reactive power compensation, and then the total susceptance is obtained. The total value is transformed into the firing angle to trigger the thyristor semiconductor. This way implements the function of both voltage flicker and var compensation in the same time.

Step Response Analysis

Step response test is performed here to check the response time of SVC using this algorithm. Q_TCR represents the per unit of output of reactive power of TCR shown in figure 5.

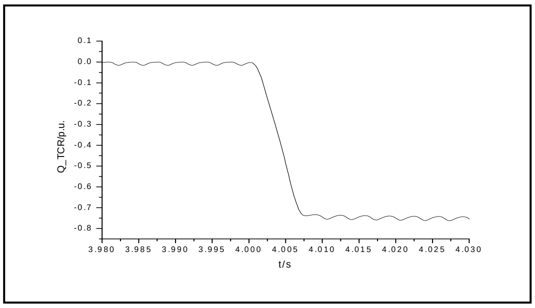


Figure 5. Step response curve of SVC

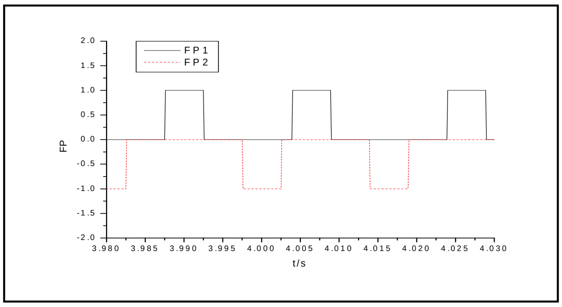


Figure 6. Firing pulse of phase AB

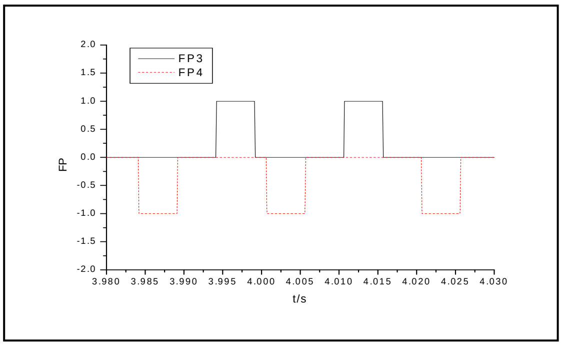


Figure 7. Firing pulse of phase BC

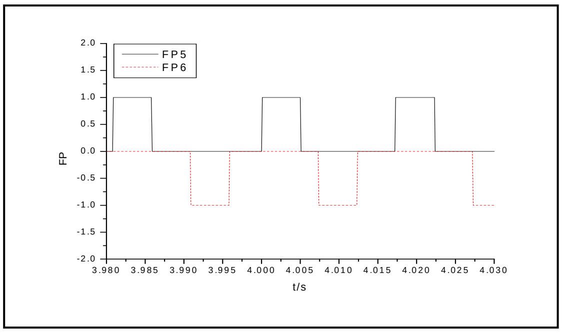


Figure 8. Firing pulse of phase CA

The figure 5 shows that the settling time is about seven milliseconds, according to the definition of IEEE 1031. The figures from 6 to 8 demonstrates that there is at least one-direction thyristor changing its firing angle in one phase bridge during the settling time. These results show that this algorithm can meet the engineering requirement upon voltage flicker reduction.

PERFORMANCE TEST

The following is one engineering example used to analyze the SVC voltage quality improvement.
There is a 110kV steel plant station in figure 9 with two 18MVA electric arc furnace on 35kV bus, and two 7MVA refining furnace on 10kV bus. The overall reactive power of electric furnace load varies seriously in the early melting processing duration, and there is often the electric furnace electrode single-phase short-circuit or two-phase short circuit, causing the supply voltage flicker. Therefore, in order to ensure the quality of power supply, an installation of the 28MVA SVC on 35kV is implemented here in the project.

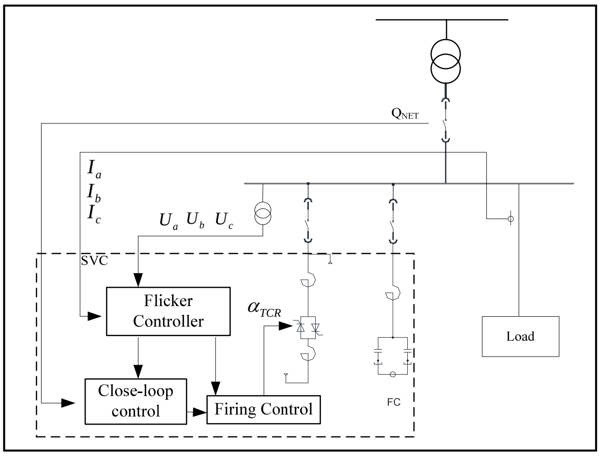


Figure 9. SVC system configuration with fast flicker reduction.

Table1 shows the maximum measured voltage flicker value before and after the SVC switching on PCC point. Results analysis show that the SVC voltage flicker improvement is more obvious with improvement rate of up to 50.3% and 50.9%. The program is governed to guarantee a long-flicker value not over 1.0.

TABLE I. VOLTAGE FLICKER MEASUREMENT VALUE

	Without SVC		
	Phase A	**Phase B**	**Phase C**
Steel melting in operation	**1.76**	**1.85**	**1.95**
	With SVC		
	Phase A	**Phase B**	**Phase C**
Steel melting in operation	**0.85**	**0.89**	**0.96**
Voltage flicker improvement rate%	**50.6**	**50.9**	**50.3**

CONCLUSION

According to the voltage flicker characteristics generated by EAF, the relationship between dynamic reactive power compensation response time and voltage flicker improvement is presented here. A rapid voltage flicker reduction algorithm with strong immunity is developed. The actual project application show that this algorithm is effective with voltage flicker improvement above fifty per cent, and SVC equipment is used with high efficiency and high engineering promotion value.

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