INFLUENCE OF VIRTUAL IMPEDANCE DESIGN AND CURRENT LIMITATION ON THE SYNCHRONIZATION OF DROOP CONTROLLED INVERTERS IN LOW VOLTAGE DISTRIBUTION SYSTEM ISLANDS WITH HIGH R/X RATIO

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ABSTRACT

A lack of knowledge on the influence of current limitation on the synchronization of droop controlled inverters in intentionally islanded distribution systems exists. As current limitation is obligatory, a severe impact would threaten the operation of inverter only islanded grids. The paper has investigated synchronization under current limitation for grid, inverter and load variations within reasonable boundaries. The effect of virtual impedances on current limitation and thereby synchronization is analyzed and compromise solutions are suggested. Further work on synchronization of practical inverter only islanded grids is proposed.

INTRODUCTION

Hierarchical control is commonly suggested for intentionally islanded operation of electrical AC low voltage (LV) distribution systems using droop control as primary control [1]. As inverter integrated decentralized generators (IIDG) are dominant in LV, a joint grid building by multiple droop controlled IIDG with voltage source behavior (DIVS) is of interest. Synchronism of the DIVS is required for continuous islanded operation. Synchronism is defined in this paper as the state of identical or marginally deviating reference frequencies of all DIVS with negligible rate of change. Synchronization is defined here as the process of regaining synchronism after a load change in the system.

In contrast to droop controlled synchronous generators (SG), each DIVS generates an individual frequency and phase angle reference based on its injected power [2]. No rotating masses exist in a DIVS-only island. Therefore, no physically determined synchronizing moments occur. Synchronization of DIVS-based islands is solely based on primary control by the droop. This differs from synchronization in e.g. transmission systems.

Success of synchronization is typically investigated in terms of small signal stability of the droop control. The frequency droop is known to be of dominant influence on droop control stability. Requirements for the droop control parameter setting are established that help enable a stable droop control [3]. Still, small signal models cannot consider saturation effects, e.g. current limitation.

From a large signal point of view synchronism is proven to be reached for inductively coupled DIVS whenever the involved power flows are physically feasible [4]. Implicitly, numerous studies based on time domain simulation have shown successful synchronization of DIVS-based islands. The DIVS under study are typically of almost identical size, design and parameterization. Often only a single grid situation is considered. The inverter side current limitation (CL), necessary due to self-protection of the IIDG, is generally not modelled. As an activated current limitation switches the DIVS from voltage to current source behavior and limits the injectable powers, an influence on synchronization is foreseeable. Furthermore, the coupling impedance, DIVS-size and load combinations activating current limitation during synchronization are unknown.

The concept of virtual impedances (VI) is often used for power sharing improvement and decoupling purposes in islands with high R/X ratios. It influences the effective coupling impedances and needs to be considered for synchronization [5].

The paper aims to identify the key factors influencing synchronization of droop controlled inverter only islands considering current limitation and virtual impedances.

MODELLING & METHODOLOGY

A large signal time domain simulation model is used in order to consider the nonlinear actuator saturation due to current limitation of DIVS. A two inverter, common load bus grid is used (Figure 1).

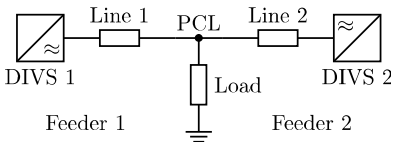


Figure 1: Study grid with Point of Common Load (PCL)

The three phase four wire coupling lines are modelled as symmetrical π-elements with reduced neutral ($R/X \approx 2.5$). The load is modelled as a symmetrical star-connected resistive constant impedance.

The island is black-started at $t = 0\,s$ in a no-load, no-voltage condition. The droop control is activated at $t = 0.1\,s$ ramping up the voltage amplitude reference until $t = 0.3\,s$. At $t = 2\,s$ load jumps are introduced by switching on the load impedances via a breaker.

As previously defined, the DIVS are droop controlled and have grid supporting voltage source behavior. The inverter bridge is modelled using the average modelling approach of [6]. Constant DC-link voltages are assumed, neglecting the primary energy source and DC-link dynamics. A fully modeled LCL-filter allows investigating

the grid side inductor influence as part of the coupling impedance. Low-pass behavior of modulation, measurements and signal processing have been neglected in order to avoid LCL-resonance occurrence since the design of LCL-damping is considered out of the scope of this paper. A one step delayed measurement feedback is used to avoid algebraic loops.

Controllers are modelled in continuous time domain. The control structure of voltage and current control follows Fig. 1 of [2]. Only fundamental frequency control is considered. The controller parameters are given in Table 1.

Table 1: Controller Parameters

Controller	k_p	k_r	ω_c
Voltage	1	4	10rad/s
Current	2	5	10rad/s

Control variables are the inverter side currents and capacitor voltages. Proportional voltage feed forward is added [6]. Current limitation (CL) is accomplished by the following approach. The current reference generated by the voltage controller is limited using the structure proposed in Figure 2 per phase in the natural reference frame.

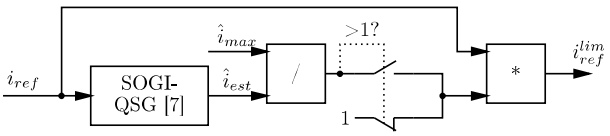


Figure 2: Used current reference limitation approach

The resulting limited current reference is of reduced amplitude but follows the unlimited reference phase angle. Temporal zero sequence references may occur until the amplitude estimation by the SOGI-QSG [7] is settled. Backtracking anti-windup with $k = 1$ is applied to the voltage controller input.

Grid side currents and capacitor voltages are used for power calculation based on instantaneous values. First order low pass filters (LPF) are used as decoupling delays with a time constant $T = 400\,ms$ for measured active and reactive power. Droop control and reference voltage calculation follows Fig. 5 in [2]. A constant proportional active power deviation feed forward onto the reference angle is used for damping. Droop constants are set assuming $|P_{max}| = |2Q_{max}| = |S_r|$ according to [1]. Setpoints are Δf_{max} = 2 Hz, ΔU_{max} = 10 V, f_0= 50 Hz, $P_0 = 0$, $Q_0 = 0$ and $U_0 = 1.05\,U_r$.

The applied structures and parameterization of fundamental frequency virtual impedances are discussed later.

The model is implemented in Matlab/ Simulink/ SimPowerSystems. The "ode4" solver is used with a fixed step width of 50 μs.

To reflect the expected diversity of grid and DIVS configurations of a real distribution system, parameters are varied simultaneously according to Table 2.

The design of experiments is performed by a global sensitivity analysis method. A radial Morris approach as described in [8] is used.

The full bandwidth of filter element p.u.-values found in reviewed literature is used. By rejection sampling resonance frequencies f_{res} are ensured to be in the range $10 f_n = 500$ Hz $< f_{res} <$ 5 kHz $= ½\, f_{sw}$ also considering a realistic bandwidth of the island's coupling line inductivities.

Table 2: Parameter variations

Parameter	**Feeder/DIVS 1**	**Feeder/DIVS 2**
Rated Power S_r	10-100 kVA	0.1-3.0 p.u. of 1
Filter $L_1\omega_n$	0.1 p.u. of Z_B	
$L_2\omega_n$	0.01-0.10 p.u. of Z_B	0.1-5.0 p.u. of 1
$C_f\omega_n$	0.01-0.15 p.u. of $1/Z_B$	0.1-5.0 p.u. of 1
Damping Term	0.05-0.15 p.u. of mP	0.8-1.2 p.u. of 1
Line length	0.05-0.30 km	0.2-2.0 p.u. of 1
Common Load	0.1-1.2 p.u. of $S_{r,1} + S_{r,2}$	
$Z_B = U_n/I_n$	$\omega_n = 2\,\pi$ 50 rad/s	

The Simulink model parameters and structure are modified by a suitable toolbox [9].

SYNCHRONIZATION WITHOUT CURRENT LIMITATION OR VIRTUAL IMPEDANCES

After a load step a transient sag of the capacitor voltages is observed to occur (**Figure 3**).

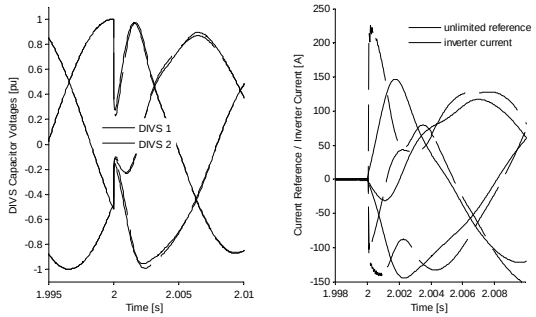


Figure 3: Initial capacitor voltages sag in each phase (left), Current reference overshot vs. actual inverter current of one DIVS per phase (right)

The depth of the sag is only slightly depending on the load step height. The observed rapid sag is ascribed to a discharging process of the filter capacities over the coupling impedances and the load. The unlimited current reference generated by the voltage controller shows a transient peak (Figure 3). It is expected to be less prominent when the low pass character of the voltage measurement feedback loop is accurately modelled. The actual inverter current may not follow the generated reference due to its low-pass character (Figure 3).

The initial current of a DIVS is defined as the amplitude of the current expected to flow after a load jump when the whole system except the droop control could react instantaneously (dots in Figure 4).

The relative height of the initial current injection following a load step has been observed to differ between the participating DIVS when grid parameters, DIVS sizing

and filter parameters are varied. Figure 4 gives an example of strongly deviating initial currents.

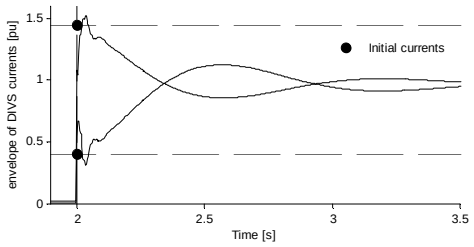
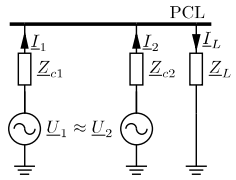


Figure 4: Example initial current ratio

For a load step from no-load condition expected initial currents of the DIVS have been observed to be explainable by the simplified model in Figure 5.



a)

$$\underline{Z}_p = \underline{Z}_{c,1} || \underline{Z}_{c,2}$$

$$\underline{I}_i = \frac{\underline{U}_i}{\underline{Z}_{c,i}} \frac{1}{1 + \frac{\underline{Z}_L}{\underline{Z}_p}}$$

b)

Figure 5: Model for expected initial currents

Due to the LPF of the droop, the droop reference angle difference may not jump. The resulting initial currents injected by the DIVS without current limitation therefore follow the above current divider model. They are mainly influenced by their coupling impedance ratio (Figure 6).

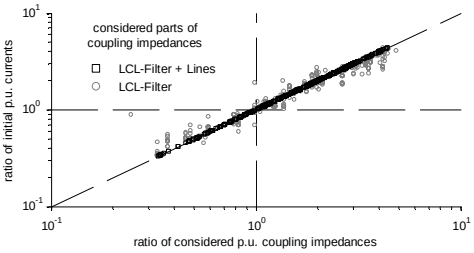


Figure 6: Ratio of initial p.u. currents based on model Fig. 4 (p.u. basis: nominal current, Z_B of DIVS).

The initial current ratio is equal for identical overall coupling impedances. According simulations verify the assumption. When considering only the filter impedance the relative error of prediction lies within ± 50 %.
Figure 7 shows the expected initial current ratio of the DIVS for the variation of parameters in Table 2. For initial currents without CL higher than the maximum DIVS current CL will occur.
Without CL or VI all simulated parameter combinations lead to successful synchronization following a load step.

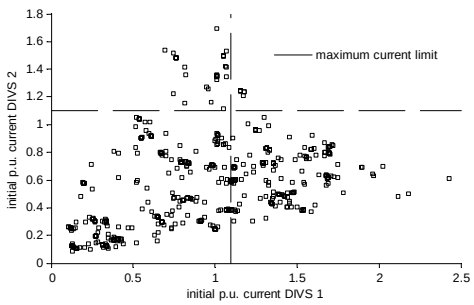


Figure 7: Initial current ratios for situations in **Table 2**

INFLUENCE OF CURRENT LIMITATION

The CL strategy limits the current reference peak due to the transient voltage sag. No significant influence on synchronization has been observed without additional initial current reference limitation.

Experiments show four combinations of initial current limitation depending on the load step height (Figure 8).

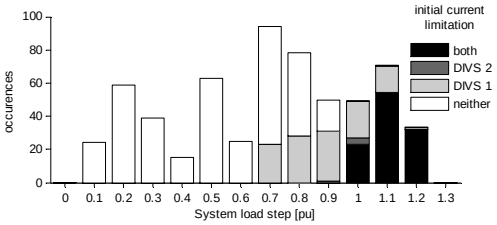


Figure 8: Initial CL for different load step heights

CL of one DIVS occur for load steps as from 0.7 p.u. due to strongly deviating initial currents. Initial CL of both DIVS is observed as from load steps of 1.0 p.u.
In comparison to the expected dominant CL of one DIVS according to Figure 7 a larger number of situations experiencing initial CL of both DIVS occurs. This is observed to occur when current injections of a DIVS A with CL and a DIVS B (at first) without CL drive a PCL voltage enforcing a power flow of B exceeding its maximum current.

The impact of initial current reference limitation on synchronization becomes evident from Figure 9.

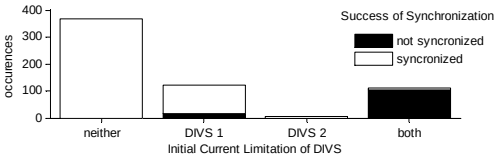


Figure 9: Success of synchronization for different initial CL combinations in Figure 8

The majority of situations with both DIVS initially current limited fails to synchronize. Due to current limitation both DIVS behave as current sources injecting a current of fixed amplitude. The residual voltages result from superposition of the injected currents at the common load and the voltages along the coupling impedances. The injected powers per DIVS are then determined by the overall system behavior. The synchronization will succeed if the injected powers coincidentally are suitable for the given grid, load and DIVS situation.
The synchronization for one initially current limited DIVS is observed to fail when the second DIVS also

enters CL after several 10-100 ms. The initial current source's and the voltage source's injected powers lead to a reference angle displacement of the droop controllers. In some cases this drives the power injection of DIVS without CL beyond its maximum current limit.
Following a load step the DIVS fail to synchronize in the majority of cases when:

1. DIVS are both initially current limited or
2. the initial CL of one DIVS leads to a CL of both

Case 1 is observed to typically happen for load steps that fully load or overload the DIVS (≥1.0 p.u.). In some cases lower loads (e.g. 0.9 p.u.) fail to synchronize due to reason 2.

INFLUENCE OF VIRTUAL IMPEDANCES

Virtual impedances (VI) modify the apparent coupling impedances of DIVS. Their effect on CL is analyzed in the following.
A common VI design for implementing partially inductive fundamental frequency VI is the stationary reference frame based approach ($\alpha\beta$-VI) [2]. It avoids differentiation and shows proportional behavior. Small time constants are introduced by measurement delays and signal processing. The apparent coupling impedance takes effect almost immediately.
Asymmetrical load currents can be shown to create a parasitic negative sequence voltage modification. With measured sequence current components $i = [i^+, i^-, i^0]^T$ the $\alpha\beta$-VI yields a negative sequence voltage modification of opposite reactive sign:

$$\Delta v = [(R + j\omega L)i^+, (R - j\omega L)i^-, 0 \cdot i^0]^T.$$

Time domain sequence extraction for separate VI application per current sequence component inevitably introduces a delay. The sequence detector proposed in [5] uses a delay constant of twice the droop decoupling LPF time constant. The DDSRF-VI approach in Figure 10 is proposed as a design variant with potentially lower time constant.

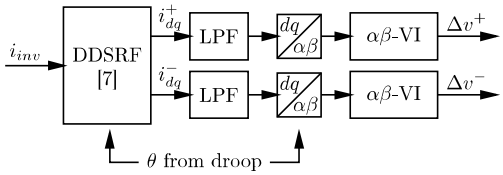


Figure 10: DDSRF-VI with LPF of time constant T

Different strategies for the parameterization of fundamental frequency VI are used.
For decoupling purposes a dominantly inductive or resistive VI is sought. This is not always achievable for larger DIVS due to observed improper voltage reduction by VI or loss of small signal stability. The latter is ascribed to LCL-resonance frequencies being reduced to near fundamental frequency by large inductive VI.
For increasing the stationary power sharing quality it is concluded from [10] and [11] that equalization of coupling impedances $\underline{Z}_{c,i} = R_{c,i} + jX_{c,i}$ following formula (1) is desirable.

$$S_j R_{c,j} = S_k R_{c,k} \;\hat{}\; S_j X_{c,j} = S_k X_{c,k} \qquad (1)$$

In this study approach (1) is used assuming full knowledge of all system parameters. Only non-negative resistive and inductive VI-components are applied.
For parameterizing the delay time constants T of the DDSRF-VI, simulations without CL under variation of T have been performed. Several cases with loss of small signal stability have been observed for T ≤ 50 ms.

As CL has been identified as a major factor on success of synchronization, the influence of VI on CL is discussed. The strategies in **Table 3** have been compared.

Table 3: Investigated Virtual Impedance strategies

Name	Current Limitation	VI Design	Delay
no VI	yes	none	-
$\alpha\beta$-VI	yes	$\alpha\beta$-VI	-
VI-100ms	yes	DDSRF-VI	100 ms
VI-400ms	yes	DDSRF-VI	400 ms

The introduction of $\alpha\beta$-VI is observed to equalize the DIVS initial current ratio and avoid the accompanying CL. The strategies VI-100ms and VI-400ms have no impact on the initial current ratio (Figure 11). For all strategies and cases with successful synchronization the stationary reactive power sharing is improved.

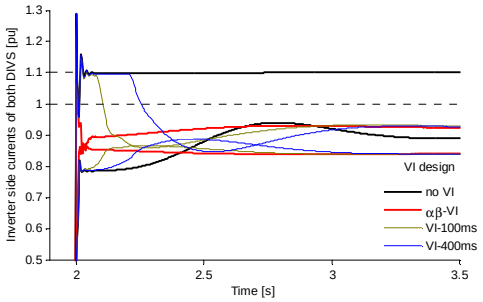


Figure 11: Example current envelopes for different VI strategies with identical DIVS, grid and load jump situation

Figure 12 shows the ability to avoid initial CL of one DIVS for all load steps ≤1p.u. by $\alpha\beta$-VI.

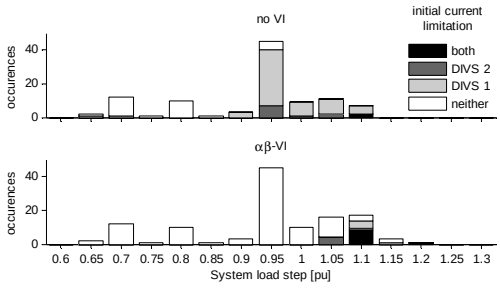


Figure 12: Initial current limitation of synchronized situations with no VI (upper) and with $\alpha\beta$-VI (lower)

The amount of situations with dual initial CL and failure of synchronization is reduced by all VI designs, most significantly by undelayed VI (Figure 13). For the latter, the ratio of successfully synchronizing situations is furthermore strongly increased.

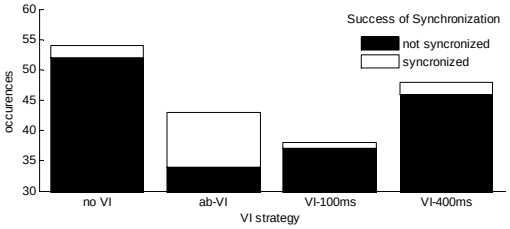


Figure 13: Success of synchronization for initial CL of both DIVS resulting for different VI strategies

The effect in case of undelayed VI is ascribed to avoidance of one-sided initial currents resulting in current limitation of the corresponding DIVS with accompanying voltage sag and in the following CL of the other DIVS.
As a compromise between positive sequence extraction and initial current equalization a parallel system of $\alpha\beta$-VI and DDSRF-VI is proposed (Figure 14). The Hybrid-VI eliminates the parasitic negative sequence voltage modification of the $\alpha\beta$-VI with a tunable delay.

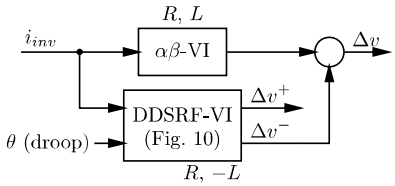


Figure 14: Suggested Hybrid-VI

Its performance will need to be investigated under asymmetrical load conditions.

CONCLUSION

The initial current ratio of two grid supporting droop controlled IIDG with voltage source behavior (DIVS) after a load jump mainly depends on their effective coupling impedance ratio. This may lead to current limitation of one or both DIVS for higher load levels. Without current limitation success of synchronization is generally observed. It is therefore a major factor for synchronization. When current limitation of both DIVS initially exists or develops, success of synchronization is critically threatened. Undelayed stationary reference frame virtual impedances may contribute to equalization of the initial current ratio. They reduce the amount of cases with initial current limitation and reduce the risk of loss of synchronization up to system loadings of 1 p.u. As virtual impedances suitable for asymmetrical loads introduce a delay they may not influence the initial current ratio. A hybrid virtual impedance has been suggested. Further work is suggested on reflecting the diversity of control aspect designs and parameterization in practical distribution systems. The feasibility of a parameterization of virtual impedances as applied here should be verified in the context of LCL-resonances and active damping. The influence of primary energy resource dynamics on synchronization under current limitation should be investigated. Further load situations should be analyzed.

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